TrenchMOS ${ }^{\text {TM }}$ transistor
Logic level FET

## GENERAL DESCRIPTION

N -channel enhancement mode logic level field-effect power transistor in a plastic envelope using 'trench' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2 kV . It is intended for use in automotive and general purpose switching applications.

PINNING - TO220AB

| PIN | DESCRIPTION |
| :---: | :--- |
| 1 | gate |
| 2 | drain |
| 3 | source |
| tab | drain |

QUICK REFERENCE DATA

| SYMBOL |  | PARAMETER | MAX. |
| :--- | :--- | :---: | :---: |
|  | UNIT |  |  |
|  | Drain-source voltage | 30 | V |
| $\mathrm{I}_{\mathrm{DS}}$ | Drain current (DC) | 75 | A |
| $\mathrm{P}_{\text {tot }}$ | Total power dissipation | 187 | W |
| $\mathrm{~T}_{\mathrm{j}}$ | Junction temperature | 175 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ | Drain-source on-state | 6 | $\mathrm{~m} \Omega$ |
|  | resistance $\quad \mathrm{V}_{\mathrm{GS}}=5 \mathrm{~V}$ |  |  |

PIN CONFIGURATION
SYMBOL



## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {DS }}$ | Drain-source voltage |  |  | 30 | V |
| $\mathrm{V}_{\text {DGR }}$ | Drain-gate voltage | $\mathrm{R}_{\mathrm{GS}}=20 \mathrm{k} \Omega$ |  | 30 | V |
| $\pm \mathrm{V}_{\text {GS }}$ | Gate-source voltage |  |  | 10 | V |
| $\mathrm{I}_{\mathrm{D}}$ | Drain current (DC) | $\mathrm{T}_{\mathrm{mb}}=25^{\circ} \mathrm{C}$ |  | 75 | A |
| $\mathrm{I}_{\mathrm{D}}$ | Drain current (DC) | $\mathrm{T}_{\mathrm{mb}}=100{ }^{\circ} \mathrm{C}$ |  | 53 | A |
| $\mathrm{D}_{\mathrm{DM}}$ | Drain current (pulse peak value) | $\mathrm{T}_{\mathrm{mb}}=25^{\circ} \mathrm{C}$ |  | 240 | A |
| $\mathrm{P}_{\text {tot }}$ | Total power dissipation | $\mathrm{T}_{\mathrm{mb}}=25^{\circ} \mathrm{C}$ |  | 187 | W |
| $\mathrm{T}_{\text {stg }}, \mathrm{T}_{\mathrm{j}}$ | Storage \& operating temperature |  | 55 | 175 | ${ }^{\circ} \mathrm{C}$ |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | TYP. | MAX. | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{R}_{\text {th } j \text {-mb }}$ | Thermal resistance junction to mounting base |  | - | 0.8 | K/W |
| $\mathrm{R}_{\mathrm{th} \mathrm{j}-\mathrm{a}}$ | Thermal resistance junction to ambient | in free air | 60 | - | K/W |

## ESD LIMITING VALUE

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
| :--- | :--- | :--- | :---: | :---: | :---: |
| V $_{\mathrm{C}}$ | Electrostatic discharge capacitor <br> voltage, all pins | Human body model <br> $(100 \mathrm{pF}, 1.5 \mathrm{k} \Omega)$ | - | 2 | kV |

TrenchMOS ${ }^{\text {TM }}$ transistor

## STATIC CHARACTERISTICS

## $\mathrm{T}_{\mathrm{j}}=25^{\circ} \mathrm{C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {(BR) }{ }^{\text {d }} \text { ( }}$ | Drain-source breakdown voltage | $\mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V} ; \mathrm{I}_{\mathrm{D}}=0.25 \mathrm{~mA} ; \mathrm{T}_{\mathrm{i}}=-55^{\circ} \mathrm{C}$ | $\begin{aligned} & 30 \\ & 27 \end{aligned}$ | - | - | V |
| $\mathrm{V}_{\text {GS(TO) }}$ | Gate threshold voltage | $\mathrm{V}_{\mathrm{DS}}=\mathrm{V}_{\mathrm{GS}} ; \mathrm{I}_{\mathrm{D}}=1 \mathrm{~mA}$ | 1.0 | 1.5 | 2.0 | V |
|  |  | $\mathrm{T}_{\mathrm{j}}=175^{\circ} \mathrm{C}$ $\mathrm{T}_{\mathrm{i}}=-55^{\circ} \mathrm{C}$ | 0.5 | - | 2.3 | V |
| $\mathrm{I}_{\text {DS }}$ | Zero gate voltage drain current | $\mathrm{V}_{\mathrm{DS}}=30 \mathrm{~V} ; \mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V}$; | - | 0.05 | 10 | $\mu \mathrm{A}$ |
|  |  | $\mathrm{V}^{\prime}=+5 \mathrm{~V} \cdot \mathrm{~V}=0 \mathrm{~V} \quad \mathrm{~T}_{\mathrm{j}}=175^{\circ} \mathrm{C}$ |  | 0.02 | 500 | $\mu \mathrm{A}$ |
| $I_{\text {gss }}$ | Gate source leakage current | $\mathrm{V}_{\mathrm{GS}}= \pm 5 \mathrm{~V} ; \mathrm{V}_{\mathrm{DS}}=0 \mathrm{~V}$ | - | 0.02 | 1 | $\mu \mathrm{A}$ |
| $\pm \mathrm{V}_{\text {(BR) }{ }^{\text {GSs }}}$ | Gate-source breakdown | $\mathrm{I}_{\mathrm{G}}= \pm 1 \mathrm{~mA}$; | 10 | - | - | $\checkmark$ |
| $\mathrm{R}_{\text {DS(ON) }}$ | Drain-source on-state resistance | $\mathrm{V}_{\mathrm{GS}}=5 \mathrm{~V} ; \mathrm{I}_{\mathrm{D}}=25 \mathrm{~A} \quad \mathrm{~T}_{\mathrm{j}}=175^{\circ} \mathrm{C}$ | - | 5 | $\begin{gathered} 6 \\ 11 \\ \hline \end{gathered}$ | $\begin{gathered} \mathrm{m} \Omega \\ \mathrm{~m} \Omega \end{gathered}$ |

## DYNAMIC CHARACTERISTICS

$\mathrm{T}_{\mathrm{mb}}=25^{\circ} \mathrm{C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{g}_{\mathrm{ts}}$ | Forward transconductance | $\mathrm{V}_{\text {DS }}=25 \mathrm{~V} ; \mathrm{I}_{\mathrm{D}}=25 \mathrm{~A}$ | 20 | 40 | - | S |
| $\begin{aligned} & \mathrm{Q}_{\mathrm{g}(\text { (tot) }} \\ & \mathrm{Q}_{\mathrm{gs}} \\ & \mathrm{Q}_{\mathrm{gd}} \end{aligned}$ | Total gate charge Gate-source charge Gate-drain (Miller) charge | $\mathrm{I}_{\mathrm{D}}=75 \mathrm{~A} ; \mathrm{V}_{\mathrm{DD}}=24 \mathrm{~V} ; \mathrm{V}_{\mathrm{GS}}=5 \mathrm{~V}$ |  | $\begin{aligned} & 92 \\ & 10 \\ & 36 \end{aligned}$ | - | $\begin{aligned} & \hline \mathrm{nC} \\ & \mathrm{nC} \\ & \mathrm{nC} \\ & \hline \end{aligned}$ |
| $\begin{aligned} & \mathrm{C}_{\mathrm{iss}} \\ & \mathrm{C}_{\text {coss }} \\ & \mathrm{C}_{\text {s }} \end{aligned}$ | Input capacitance Output capacitance Feedback capacitance | $\mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V} ; \mathrm{V}_{\mathrm{DS}}=25 \mathrm{~V} ; \mathrm{f}=1 \mathrm{MHz}$ |  | $\begin{aligned} & \hline 5000 \\ & 1150 \\ & 500 \end{aligned}$ | - | $\begin{aligned} & \mathrm{pF} \\ & \mathrm{pF} \\ & \mathrm{pF} \end{aligned}$ |
| $\begin{aligned} & \mathrm{t}_{\mathrm{t} \text { on }} \\ & \mathrm{t}_{\mathrm{t}} \\ & \mathrm{t}_{\mathrm{d} \text { of }} \end{aligned}$ | Turn-on delay time <br> Turn-on rise time Turn-off delay time Turn-off fall time | $\mathrm{V}_{\mathrm{DD}}=15 \mathrm{~V} ; \mathrm{I}_{\mathrm{D}}=25 \mathrm{~A} ;$ <br> $\mathrm{V}_{\mathrm{GS}}=5 \mathrm{~V} ; \mathrm{R}_{\mathrm{G}}=5 \Omega$ <br> Resistive load |  | $\begin{gathered} 45 \\ 120 \\ 225 \\ 150 \\ \hline \end{gathered}$ | $\begin{gathered} 60 \\ 170 \\ 300 \\ 135 \end{gathered}$ | $\begin{aligned} & \mathrm{ns} \\ & \mathrm{~ns} \\ & \mathrm{~ns} \\ & \mathrm{~ns} \end{aligned}$ |
| L L $L_{\text {d }}$ $L_{\text {d }}$ | Internal drain inductance Internal drain inductance Internal source inductance | Measured from contact screw on tab to centre of die <br> Measured from drain lead 6 mm from package to centre of die Measured from source lead 6 mm from package to source bond pad | - | 3.5 4.5 7.5 | - | nH nH nH |

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REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS
$\mathrm{T}_{\mathrm{j}}=25^{\circ} \mathrm{C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{I}_{\mathrm{DR}}$ | Continuous reverse drain |  |  | - | 75 | A |
| $\mathrm{I}_{\text {dRM }}$ | Pulsed reverse drain current |  |  | - | 240 | A |
| $\mathrm{V}_{\text {SD }}$ | Diode forward voltage | $\begin{aligned} & I_{F}=25 \mathrm{~A} ; \mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{F}}=75 \mathrm{~A} ; \mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V} \end{aligned}$ | - | $\begin{gathered} 0.85 \\ 1.0 \end{gathered}$ | 1.2 | V |
| $\begin{array}{\|l\|l} \mathrm{t}_{\mathrm{Q}} \\ \mathrm{Q}_{\mathrm{r}} \end{array}$ | Reverse recovery time Reverse recovery charge | $\begin{aligned} & \mathrm{I}_{\mathrm{F}}=75 \mathrm{~A} ;-\mathrm{d} \mathrm{I}_{\mathrm{F}} / \mathrm{dt}=100 \mathrm{~A} / \mu \mathrm{s} ; \\ & \mathrm{V}_{\mathrm{GS}}=-10 \mathrm{~V} ; \mathrm{V}_{\mathrm{R}}=25 \mathrm{~V} \end{aligned}$ |  | $\begin{aligned} & 100 \\ & 0.6 \end{aligned}$ | - | $\begin{aligned} & \mathrm{ns} \\ & \mu \mathrm{C} \end{aligned}$ |

## AVALANCHE LIMITING VALUE

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| W $_{\text {DSS }}$ | Drain-source non-repetitive <br> unclamped inductive turn-off <br> energy | $\mathrm{I}_{\mathrm{D}}=75 \mathrm{~A} ; \mathrm{V}_{\mathrm{DD}} \leq 15 \mathrm{~V} ;$ <br> $\mathrm{V}_{\mathrm{GS}}=5 \mathrm{~V} ; \mathrm{R}_{\mathrm{GS}}=50 \Omega ; \mathrm{T}_{\mathrm{mb}}=25^{\circ} \mathrm{C}$ | - | - | 500 | mJ |

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Fig. 1. Normalised power dissipation. $P D \%=100 \cdot P_{D} / P_{D 25^{\circ}}{ }^{\circ}=f\left(T_{m b}\right)$


Fig.2. Normalised continuous drain current. $I D \%=100 \cdot I_{D} / I_{D 25}{ }^{\circ}=f\left(T_{m b}\right)$; conditions: $V_{G S} \geq 5 \mathrm{~V}$


Fig.3. Safe operating area. $T_{m b}=25^{\circ} \mathrm{C}$ $I_{D} \& I_{D M}=f\left(V_{D S}\right) ; I_{D M}$ single pulse; parameter $t_{p}$


Fig.4. Transient thermal impedance.
$Z_{\text {th } j-m b}=f(t) ;$ parameter $D=t_{p} / T$


Fig.5. Typical output characteristics, $T_{j}=25^{\circ} \mathrm{C}$. $I_{D}=f\left(V_{D S}\right)$; parameter $V_{G S}$


Fig.6. Typical on-state resistance, $T_{j}=25^{\circ} \mathrm{C}$. $R_{D S(O N)}=f\left(I_{D}\right)$; parameter $V_{G S}$

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 BUK9506-30

Fig.7. Typical transfer characteristics. $I_{D}=f\left(V_{G S}\right)$; conditions: $V_{D S}=25 \mathrm{~V}$; parameter $T_{j}$


Fig.8. Typical transconductance, $T_{i}=25^{\circ} \mathrm{C}$. $g_{t s}=f\left(I_{D}\right)$; conditions: $V_{D S}=25 \mathrm{~V}$


Fig.9. Normalised drain-source on-state resistance. $a=R_{D S(O N)} / R_{D S\left(O N / 25^{\circ} \mathrm{C}\right.}=f\left(T_{\mathrm{T}}\right) ; I_{D}=25 \mathrm{~A} ; V_{G S}=5 \mathrm{~V}$


Fig.10. Gate threshold voltage.
$V_{G S(T O)}=f\left(T_{j}\right)$; conditions: $I_{D}=1 \mathrm{~mA} ; V_{D S}=V_{G S}$


Fig.11. Sub-threshold drain current.
$I_{D}=f\left(V_{G S}\right) ;$ conditions: $T_{j}=25^{\circ} \mathrm{C} ; V_{D S}=V_{G S}$


Fig.12. Typical capacitances, $C_{i s s}, C_{\text {oss }}, C_{\text {rss. }}$. $C=f\left(V_{D S}\right) ;$ conditions: $V_{G S}=0 V ; f=1 \mathrm{MHz}$

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Fig.13. Typical turn-on gate-charge characteristics. $V_{G S}=f\left(Q_{G}\right)$; conditions: $I_{D}=75$ A; parameter $V_{D S}$


Fig.14. Typical reverse diode current. $I_{F}=f\left(V_{S D S}\right)$; conditions: $V_{G S}=0 \mathrm{~V}$; parameter $T_{j}$


Fig.15. Normalised avalanche energy rating. $W_{D S s} \%=f\left(T_{m b}\right)$; conditions: $I_{D}=75 \mathrm{~A}$


Fig.16. Avalanche energy test circuit.

$$
W_{D S S}=0.5 \cdot L I_{D}^{2} \cdot B V_{D S S}\left(\left(B V_{D S S}-V_{D D}\right)\right.
$$



Fig.17. Switching test circuit.

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## MECHANICAL DATA



Fig.18. SOT78 (TO220AB); pin 2 connected to mounting base.

## Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for SOT78 (TO220) envelopes.
3. Epoxy meets UL94 V0 at 1/8".

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## DEFINITIONS

| Data sheet status |  |
| :--- | :--- |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one <br> or more of the limiting values may cause permanent damage to the device. These are stress ratings only and <br> operation of the device at these or at any other conditions above those given in the Characteristics sections of <br> this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |
| Application information |  |
| Where application information is given, it is advisory and does not form part of the specification. |  |
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